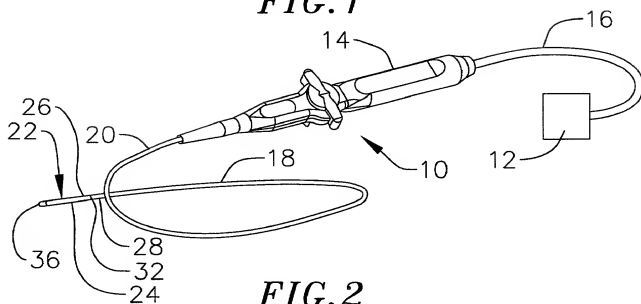
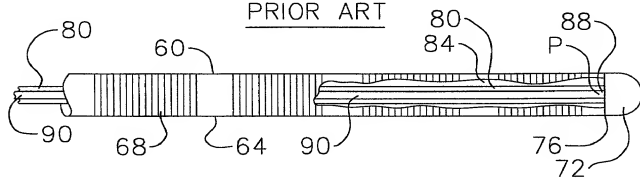


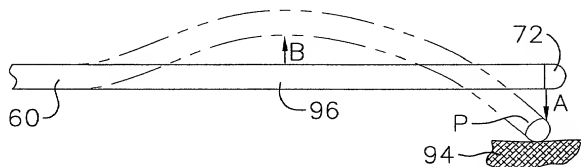
**FIG. 1**



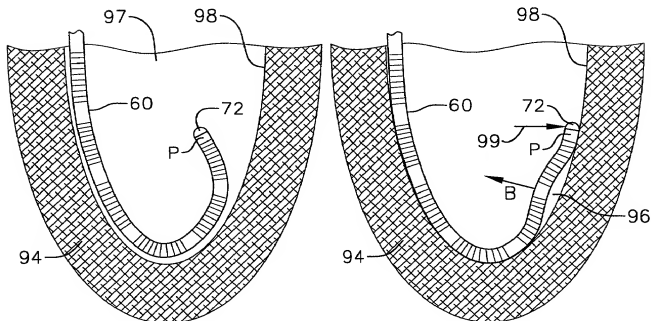
**FIG. 2**  
PRIOR ART



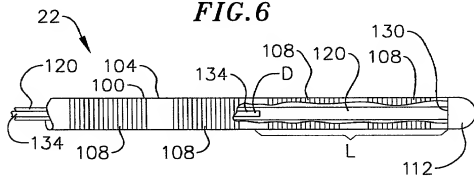
**FIG. 3**  
PRIOR ART



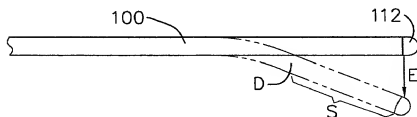
**FIG.5**  
PRIOR ART



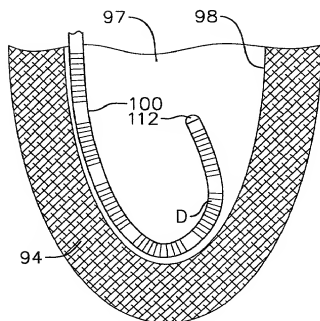
*FIG. 6*



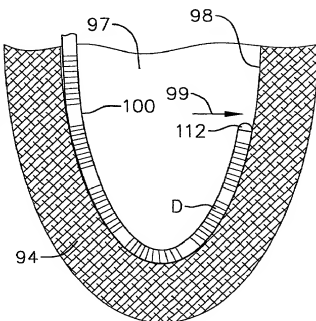
*FIG. 7*

[illegible]

**FIG. 8**



**FIG. 9**



**FIG. 10**

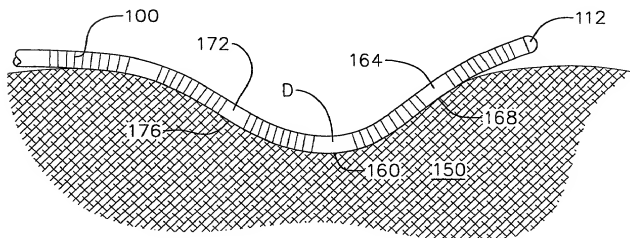


FIG. 11

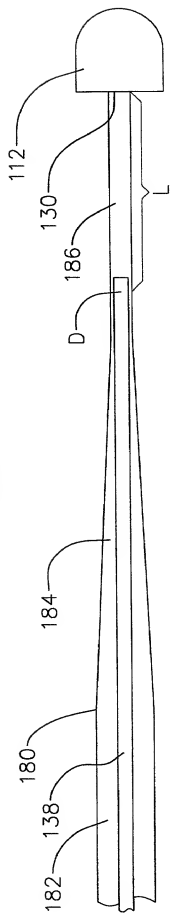
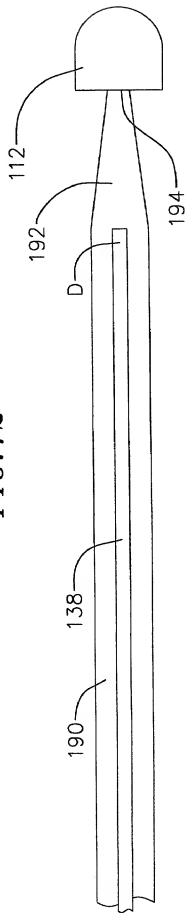
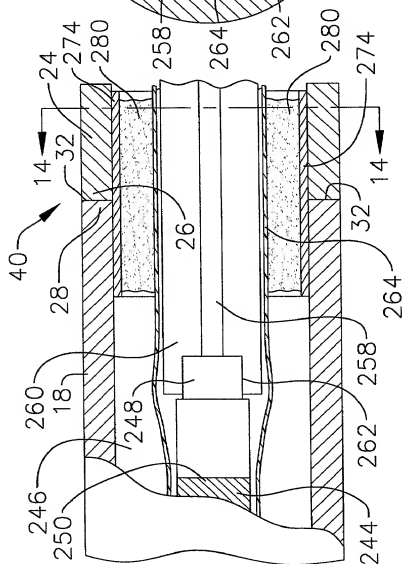


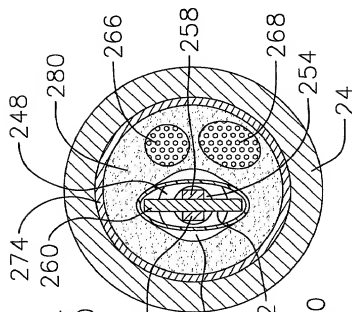
FIG. 12



**FIG. 13**  
PRIOR ART



**FIG. 14**  
PRIOR ART



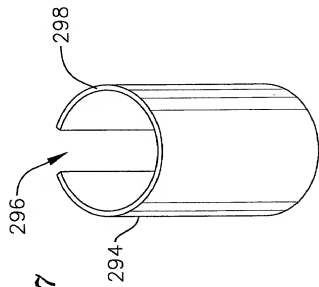
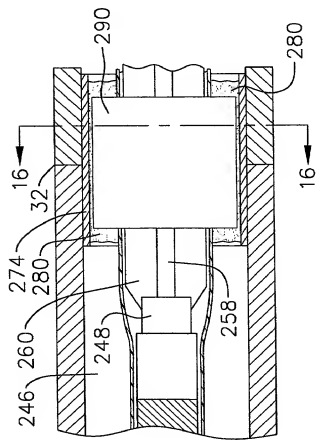
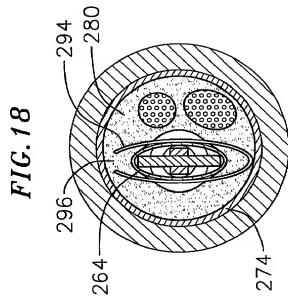
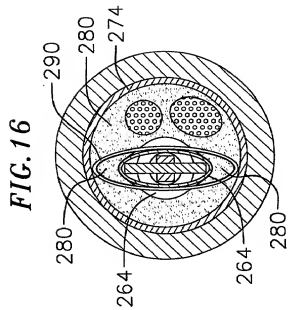


FIG. 15

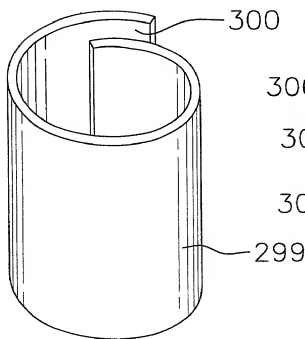
FIG. 16

FIG. 18

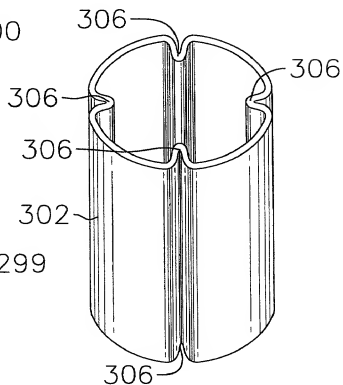
FIG. 15

FIG. 17

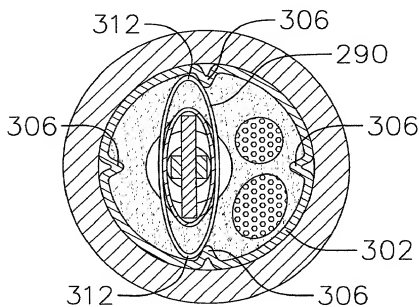
**FIG. 17A**

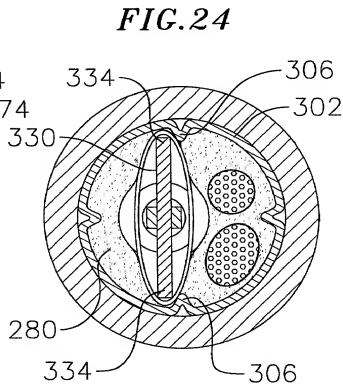
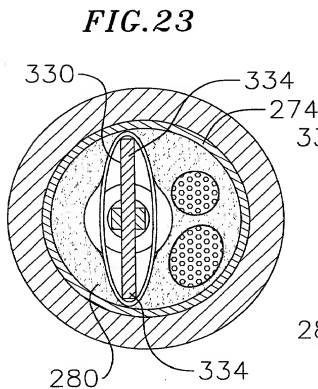
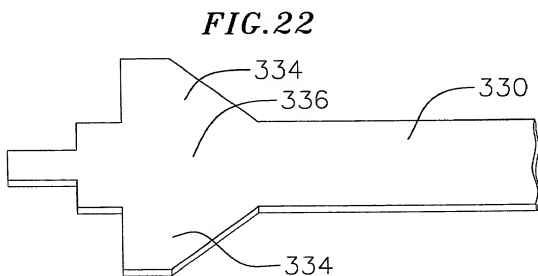
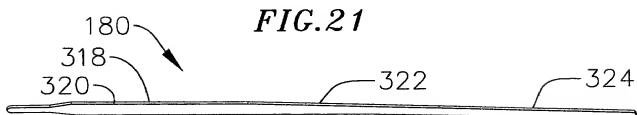


**FIG. 19**

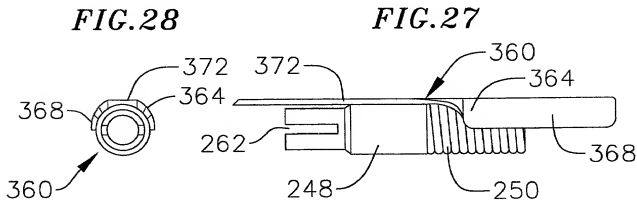
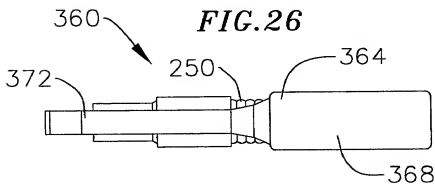
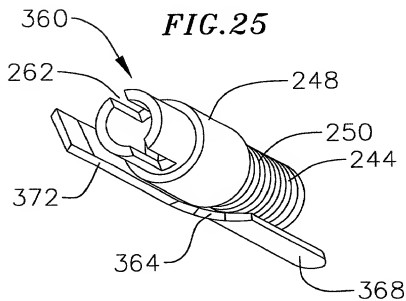


**FIG. 20**









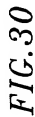
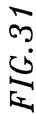
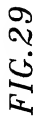


FIG. 32

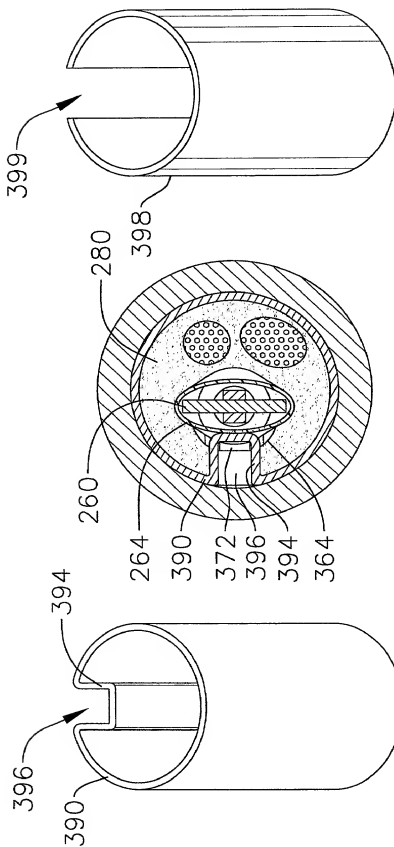


FIG. 33

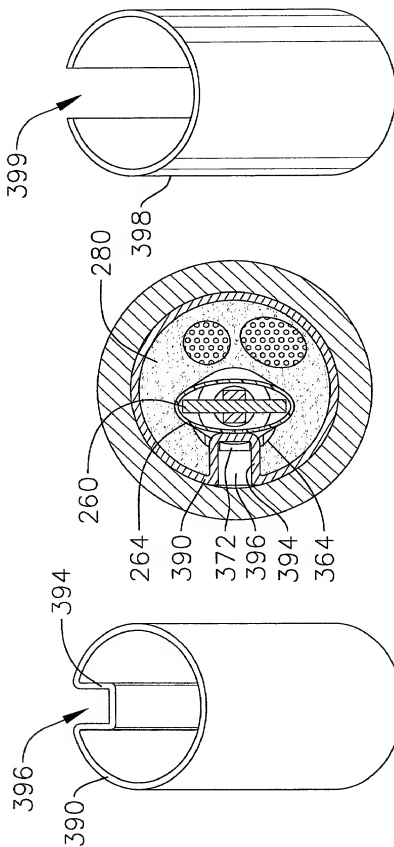
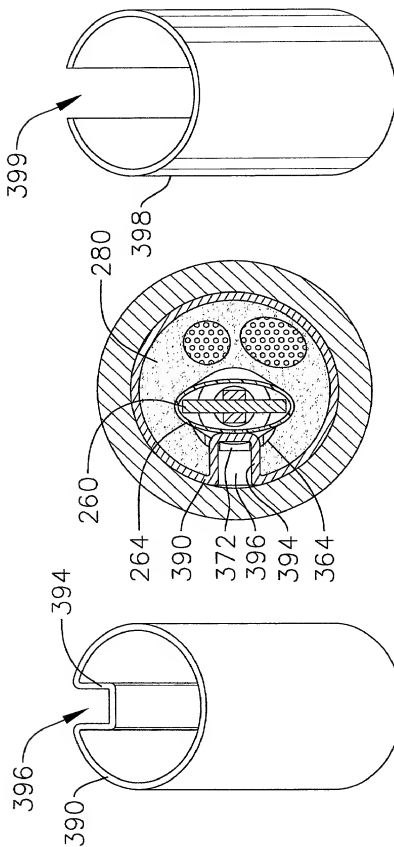


FIG. 34



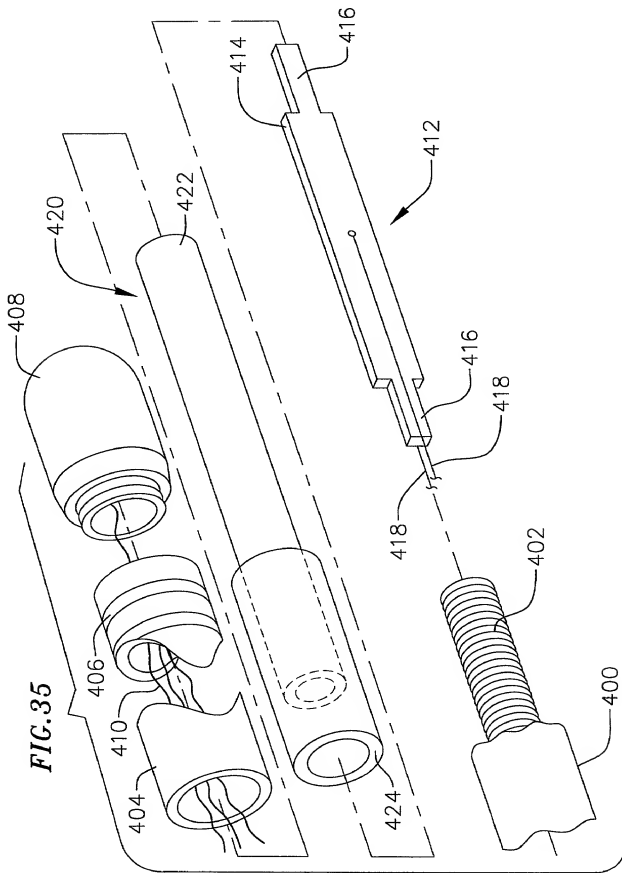


FIG. 4 is a cross-sectional view of a semiconductor device. The device includes a substrate 400, a first conductive layer 410, a second conductive layer 422, and a third conductive layer 430. A fourth conductive layer 424 is also shown. A contact pad 431 is formed on the first conductive layer 410.